What is claimed is:

1. A method of fabricating a semiconductor device that comprises a memory region including a non-volatile storage device and a logic circuit region including a peripheral circuit for the non-volatile storage device, the method comprising steps of:

(a) forming a first dielectric layer over a semiconductor layer,

(b) forming a first conductive layer over the first dielectric layer,

(c) forming a stopper layer over the first conductive layer,

(d) patterning the stopper layer and the first conductive layer within the memory region,

(e) forming a charge accumulation film over the memory region and the logic circuit region,

(f) forming a second conductive layer over the charge accumulation film, then forming control gates in the form of side walls over both side surfaces of the first conductive layer within at least the memory region with the charge accumulation film interposed in between, by anisotropic etching of the second conductive layer,

(g) forming first side wall dielectric layers on at least upper portions of the control gates and over both side surfaces of a laminate formed of the stopper layer and the first conductive layer,

(h) removing the stopper layer from within the logic circuit region,

(i) patterning the first conductive layer within the logic circuit region, to form a gate electrode of an insulated-gate field-effect transistor within the logic circuit region,

(j) forming side wall dielectric layers on both side surfaces of the gate electrode, and also forming a second side wall dielectric layer so as to cover each of the first side wall dielectric layers and each of the control gates,

(k) forming first impurity layers, each of which becomes a source region or a drain region of the non-volatile storage device and forming second impurity layers, each of

which becomes a source region or a drain region of the insulated-gate field-effect transistor,

(l) forming silicide layers on the surfaces of the first impurity layers and the second impurity layers,

(m) forming a second dielectric layer over the memory region and the logic circuit region,

(n) removing the second dielectric layer in such a manner that the stopper layer is exposed within the memory region and also the gate electrode is not exposed within the logic circuit region,

(o) removing the stopper layer from within the memory region, and

(p) patterning the first conductive layer within the memory region, to form a word gate for the non-volatile storage device within the memory region.

2. The method of fabricating a semiconductor device as defined by claim 1, wherein:

the step (l) comprises forming a silicide layer on the surface of the gate electrode.

3. The method of fabricating a semiconductor device as defined by claim 1, wherein:

in the step (n), the second dielectric layer is removed by polishing.

4. The method of fabricating a semiconductor device as defined by claim 1, wherein:

an ONO film is used as the charge accumulation film.